REMARKS

Claims 5-13 were examined and stand rejected as being anticipated by U.S. Patent Application Publication No. 2002/0089887 issued to Hii, et al. ("Hii"). Applicants respectfully disagree with the rejection for the following reasons.

Claim 5 recites a memory IC module having a carrier substrate, first and second signal connection points on the substrate, memory devices on the substrate where each has a separate memory core array and separate address decoder logic, and a memory buffer installed on the substrate between the signal connection points and the memory devices. The buffer has driver circuits whose outputs are coupled to the first signal connection points, respectively. The buffer also has logic to forward read data, provided by the memory devices, at speed and using the drivers in a normal mode of operation for the module. The logic is to also determine error in test symbols, received from outside the module at speed using the second signal connection points, in a test mode of operation for the module during which a chip-to-chip connection between the module and another device is tested. Hii does not teach or suggest such an IC module.

Hii has a built-in self-test arrangement for IC memory devices, where a logic circuit produces output signals stored by a BIST register that controls a self-test of the integrated circuit. A comparator compares expected data bits with data bits written into and read from a memory array to determine whether the integrated circuit passes or fails the test. This, however, does not teach or suggest Applicants' IC module in claim 5 in which there is a memory buffer on the substrate between signal connection points of the substrate and memory devices, and where the buffer has logic to determine error in test symbols received from outside the module at speed using signal connection points of the substrate during which a chip-to-chip connection between the module and another device is tested. Hii only describes a built-in self-test arrangement for testing the storage functionality of a single memory device, but does not teach or suggest any testing of chip-to-chip connections.

In addition, at page 3 of the Office Action does not clearly set forth the Examiner's case for rejecting the claim. For example, the Office Action refers to the claimed "carrier substrate" as being taught in the Abstract and, in particular, Fig. 1 of

Hii. However, there is no mention of any substrate in the Abstract or Fig. 1. Applicants are therefore left wondering what is the" carrier substrate" that the Office Action contends is taught. Assuming for the sake of argument that the carrier substrate is the board on which the memory devices are installed as shown in Fig. 5 of Hii, one is left again wondering what are the claimed "first and second signal connection points" which, according to Applicants' claim 5, are "on the substrate". The Office Action refers to page 1, sections 0002-005 which fill almost an entire column of text. Nowhere in this text has the Office Action pointed to where the claimed signal connection points would be taught.

A reason why the above two points are being made here is that Applicants' claimed "memory buffer" is to be communicatively coupled between the signal connection points and the memory devices. Of course, this buffer is also recited as having driver circuits whose outputs are coupled to the first signal connection points, and logic to forward read data and to determine error in test symbols received from outside the module using the second signal connection point. Other than referring to Figs. 13A-C, Fig. 1, unit 100, and unit 120, the Office Action does not explain how Applicants' claim language reads on the reference. For example, units 100 and 120 are address and control signal buffers that appear in each memory device. If these are "memory buffers", then how can they be communicatively coupled **between** the signal connection points of the substrate and the memory devices? Also, Figs. 13A-C show the interface between BIST generated signals and the main devices, a multiplex circuit which chooses between BIST generated signals B-Ax and external signals Ax from outside. If these are the "memory buffers", then what part of them "determines error in test symbols received from outside the module during a test mode"? For that, the Office Action on page 3 refers to "page 9, unit 0215-260" of Hii. However, this section only refers to algorithms for testing the storage array of the memory device and does not suggest analyzing test symbols that arrive from outside the memory device. Applicants therefore respectfully request that the Examiner clarify this rejection in the next Office Action, because as it stands now, the rejection of claim 5 does not meet the requirements of the Patent Rules for clearly setting forth the basis of the rejection.

Turning now to claim 9, this claim also stands rejected as being anticipated by Hii. Once again, Applicants respectfully disagree with the rejection, because firstly, Hii does not teach or suggest a host IC device having memory controller logic installed on a substrate. Hii only describes a built-in self-test arrangement for a memory device, to test itself. There is no suggestion of modifying a substrate having a host IC device in which memory controller logic and built-in self-test generator logic cooperate as recited in Applicants' claim 9. It should be noted that the phrase *memory controller logic* does not simply refer to any logic circuitry that performs some form of control function related to memory devices. Rather, the phrase *memory controller* has a well defined and understood meaning by those of ordinary skill in the art as referring to a circuit that allows a processor to access multiple memory devices through a single interface. The BIST arrangement of Hii is only intended to perform a self-test of each memory device itself, without regard to any memory controller. Accordingly, the rejection of claim 9 as being anticipated by Hii is also improper and should be withdrawn.

Any dependent claims not specifically mentioned above are submitted as being neither anticipated or obvious, for at least the reasons given above in support of their base claims.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

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Margaux Rodriguez *March 21, 2005*